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1 coating temperatures. *This is practicable because of special cooling*
2 *apparatus, specially located.*" (emphasis in original) 188 USPQ 358.
3 Additionally, the Mayhew Court indicates that Mayhew's specification
4 stated that if a high temperature galvanizing spelter were present in a
5 zone, "iron dissolution and dross formation would make it *impossible to*
6 *produce the smooth coat produced by the present invention.*" (emphasis in
7 original) 188 USPQ 361. As evidenced by the above-quoted sections
8 of Mayhew's specification, Mayhew unambiguously stated in his
9 specification that the recited invention required (i.e., was impossible
10 without) specific embodiments set forth by Mayhew.

11 In re Mayhew was contrasted by the Patent and Trademark Office
12 Board of Patent Interferences in Beale v. Schuman, 212 USPQ 291-294,
13 at page 293. In Beale, the Board explained that In re Mayhew was
14 inapplicable to a case in which an Applicant had provided nothing in
15 his disclosure which required claims to be confined solely to disclosed
16 embodiments.

17 Applicant's disclosure, like the disclosure at issue in Beale,
18 provides nothing to indicate that Applicant's claims are to be confined
19 solely to disclosed embodiments. Accordingly, In re Mayhew is
20 inapplicable to Applicant's claims.

21 Specifically, Applicant has not indicated that any disclosed
22 improvements are necessary to the practice of Applicant's claimed
23 invention. Rather, Applicant indicates exactly the opposite, that "[o]ne
24 or more of the [disclosed] techniques, or other techniques, can be

1 utilized in the production of 64M, 16M or 4M memory chips in
2 accordance with the invention, with the invention only being limited by
3 the accompanying claims appropriately interpreted in accordance with the
4 doctrine of equivalents." (Page 9, lines 3-7 of Applicant's specification,
5 emphasis added.) Applicant further indicates that the specifically
6 disclosed methods of achieving high device density are provided by way
7 of example only and not by way of limitation. (See, for example, page
8 37, lines 21-24; and page 39 lines 5-8). Thus, unlike the disclosure at
9 issue in Mayhew, Applicant's disclosure in no way limits Applicant's
10 claims to disclosed embodiments of Applicant's claimed devices. For at
11 least this reason, the Examiner's rejections of claims 6-10, 18-19, 22-23
12 and 25-26 under 35 U.S.C. §112, first paragraph, are improper.
13 Applicant therefore requests that such §112 rejections be withdrawn in
14 the Examiner's next action.

15 Claims 7, 9 and 10 are rejected under 35 U.S.C. §112, second
16 paragraph as being indefinite. Specifically, the Examiner rejects
17 Applicant's use of the term "composite" within the claims. The
18 Examiner contends that such term is vague and indefinite. Without
19 admission as to the propriety of the Examiner's rejection, Applicant has
20 amended claims 7, 9 and 10 to remove the word "composite" from such
21 claims. Applicant therefore requests that the rejection of claims 7, 9
22 and 10 under 35 U.S.C. §112, second paragraph, be withdrawn in the
23 Examiner's next action.
24

1 Applicant's pending claims are allowable over the prior art.

2
3 Pending claims 6-10, 18-19, 22-23 and 25-26 stand rejected under
4 35 U.S.C. § 103 as being unpatentable over Applicant's admitted prior
5 art in view of Denboer. Applicant disagrees.

6 Applicant's pending claims recite specific memory cell densities
7 which, prior to Applicant's disclosure, had not been attained by the art.
8 Nothing in either Applicant's "Background of the Invention", or Denboer
9 suggest that Applicant's specifically recited memory cell densities were
10 attained prior to Applicant's filing of the application.

11 The Examiner cites the fact that 16M DRAM chips existed in the
12 prior art prior to Applicant's filing as being evidence of the obviousness
13 of Applicant's invention. Applicant does not dispute the prior art
14 existence of 16M DRAM chips. What Applicant discloses and claims,
15 however, are 16M DRAM chips formed to higher densities than had
16 previously been disclosed by the art.

17 The Examiner correctly notes that "[m]aximizing density of a single
18 transistor and other memory cells is a continuing goal in semiconductor
19 memory fabrication," but then mischaracterizes the quoted phrase to be
20 evidence of the obviousness of Applicant's invention. The quoted phrase
21 is, in fact, evidence of the non-obviousness of Applicant's invention.
22 The quoted phrase shows that, in spite of a continuing goal of
23 maximizing density of memory cells, no one prior to Applicant to the
24 best of Applicant's knowledge, had taught a 16M DRAM chip at the

1 density disclosed and claimed by Applicant. The fact that such density
2 was a goal of persons skilled in the art which had not been achieved
3 prior to Applicant's disclosure, evidences a long-felt need by persons of
4 skill in the art to accomplish Applicant's invention. Such showing of
5 long-felt need is one of the considerations set forth in the touchstone
6 case of Graham v. John Deere for evidencing non-obviousness. (See,
7 Graham v. John Deere Co., 383 US 1 (1966).) Thus, the Examiner's
8 very quoted phrase evidences the non-obviousness of Applicant's claimed
9 invention, not the obviousness of such invention. For at least this
10 reason, claims 6-10, 18-19, 22-23 and 25-26 are allowable over the prior
11 art.

12 Referring to the individual pending claims, the claims are further
13 allowable for specifically reciting features which are neither shown nor
14 suggested by the cited art.

15 For instance, referring to claim 6, the claim specifically recites a
16 semiconductor memory device comprising from 16,000,000 to 17,000,000
17 functional and operably addressable memory cells arranged in multiple
18 memory arrays formed on a die, the individual functional and operably
19 addressable memory cells occupying an area on the die within the
20 memory arrays, the occupied area of all functional and addressable
21 memory cells on the die having a total combined area which is no
22 greater than 14 mm².

23 Nothing in the Examiner's cited prior art discloses or suggests such
24 recited semiconductor memory device. Specifically, nowhere in

1 Applicant's "Background of the Invention" is there any disclosure or
2 suggestion that it was known in the art to form from 16,000,000 to
3 17,000,000 functional and operably addressable memory cells on a die
4 having a total combined area which is no greater than 14 mm², and
5 nowhere in Denboer is there disclosure or suggestion of such recited
6 feature. As neither of the Examiner's cited references discloses or
7 suggests the recited feature of a total of from 16,000,000 to 17,000,000
8 functional operable addressable memory cells arranged in multiple
9 memory arrays formed on a die having a total combined area which is
10 no greater than 14 mm², it is inconceivable that the references could,
11 in combination suggested such recited feature. For at least this reason,
12 claim 6 is allowable over the cited references.

13 Referring to claims 7-10, these claims depend from claim 6 and
14 are therefore allowable for the reasons discussed above regarding
15 claim 6, as well as for their own recited features which are neither
16 shown nor suggested by the prior art. For instance, claim 9 recites that
17 the claim 6 recited total die area is not greater than about 11 mm².
18 It is inconceivable that references which do not even suggest a die
19 having a recited total combined area which is no greater than 14 mm²
20 could possibly suggest a die having such recited total combined area not
21 greater than 11 mm². For at least this additional reason, claim 9 is
22 allowable over the cited references. Applicant therefore requests
23 allowance of claim 9 in the Examiner's next action.
24

1 Referring to claims 18-19, 22-23 and 25-26, these claims recite
2 memory arrays containing at least one area of 100 square microns of
3 continuous die surface area having at least 128 functional and operably
4 addressable memory cells. Neither Denboer, nor Applicant's "Background
5 of the Invention" section, suggests or discloses such recited feature. As
6 neither of the Examiner's cited references suggests the recited memory
7 arrays containing at least one area of 100 square microns of continuous
8 die surface area having at least 128 functional and operably addressable
9 memory cells, it is inconceivable that references could, in combination,
10 suggest such recited feature. For at least this reason, claims 18-19, 22-
11 23 and 25-26 are allowable over the cited references.

12 Claims 19, 25 and 26 are further allowable in that the claims
13 recite memory arrays containing at least one area of 100 square microns
14 of continuous die surface area having at least 170 functional and
15 operably addressable memory cells. As discussed above, the Examiner's
16 cited references do not even suggest a recited 100 square microns of
17 continuous die surface having at least 128 functional and operably
18 addressable memory cells. Accordingly, is inconceivable that such
19 references could suggest such the recited continuous die surface having
20 at least 170 functional and operably addressable memory cells. For at
21 least this additional reason, claims 19 and 25-26 are allowable over the
22 Examiner's cited references.

23 For the above discussed reasons, claims 6-10, 18-19, 22-23 and 25-
24 26 are not obvious over the prior art. Applicant therefore requests that

1 the rejections of claims 6-10, 18-19, 22-23 and 25-26
2 under 35 U.S.C. § 103 be withdrawn in the Examiner's next action.

3
4 Applicant requests allowance of the pending claims in the Examiner's
5 next action.

6 For the above-discussed reasons, the Examiner's rejections of
7 claims 6-10, 18-19, 22-23 and 25-26 should be withdrawn, and claims 6-
8 10, 18-19, 22-23 and 25-26 allowed to issue. Applicant therefore
9 requests formal allowance of claims 6-10, 18-19, 22-23 and 25-26 in the
10 Examiner's next action.

11 Respectfully submitted,

12
13 Dated: 6/18/97

By:  #32,268 for

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